## REMARKS

This Amendment responds to the Office Action dated December 14, 2004 in which the Examiner objected to claim 6, rejected claims 1-3, 5 and 11 under 35 U.S.C. §102(b), rejected claims 8 and 10 under 35 U.S.C. §103, stated that claims 9 and 12 are allowed and objected to claim 4 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, an informality in claim 6 has been corrected. Therefore, Applicants respectfully request the Examiner withdraws the objection to claim 6.

As indicated above, claim 1 has been amended to make explicit what is implicit in the claim. The amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claim. Claims 3-5 have been amended to correspond to the amendment made to claim 1. Claims 8 and 11 have been amended for stylistic reasons. The amendments to claims 3-5, 8 and 11 are unrelated to a statutory requirement of patentability and do not narrow the literal scope of the claims.

Claim 1 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, single-stage delta-sigma modulator and output operating unit. The component separating unit separates a signal component and an error component of a digital input signal from each other. The single-stage delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the single-stage delta-sigma modulator.

Through the structure of the claimed invention having a single-stage delta-sigma modulator as claimed in claim 1, the claimed invention provides a modulator which can improve stability and precision. The prior does not show, teach or suggest the invention as claimed in claim 1.

Claim 8 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, a delta-sigma modulation and an output operating unit. The component separating unit separates a signal component and an error component of an input signal from each other. The delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the delta-sigma modulator. The component separating unit includes a first quantizer, a first digital-to-analog converter and an adder. The first quantizer quantizes an analog input signal. The first digital-to-analog converter converts the signal component provided from the first quantizer to an analog signal. The adder adds the analog input signal to the analog signal provided from the first digital-to-analog converter. The delta-sigma modulator includes a plurality of integrators, a second quantizer, a second digital-to-analog converter and a delay element. The second quantizer quantizes an output of the integrator in the final stage. The second digital-to-analog converter converts an output of the second quantizer to an analog signal. The delay element delays the analog signal provided from the second digital-to-analog converter, and performs negative feedback by sending the delayed analog signal to the plurality of integrators.

Through the structure of the claimed invention having a component separating unit include a first quantizer which quantizes an analog input signal, as claimed in claim 8, the claimed invention provides a modulator with improved stability. The prior art does not show, teach or suggest the invention as claimed in claim 8.

Claim 11 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, delta-sigma modular and output operating unit. The component separating unit separates a signal component and an error component of an analog input signal from each other. The delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the delta-sigma modulator. The component separating unit includes a multibit quantizer, digital-to-analog converter and an adder. The multibit quantizer quantizes the analog input signal to provide a multibit form. The digital-to-analog converts converting the signal component provided from the multibit quantizer to an analog signal. The adder adds the analog input signal to the analog signal provided from the digital-to-analog converter.

Through the structure of the claimed invention having a component separating unit including a multibit quantizer quantizing the analog input signal to provide a multibit form as claimed in claim 11, the claimed invention provides a modulator having improved stability. The prior art does not show, teach or suggest the invention as claimed in claim 11.

Claims 1-3 and 5 were rejected under 35 U.S.C. §102(b) as being anticipated by *Karema et al.* (U.S. Patent No. 5,061,928).

*Karema et al* appears to disclose a method of cascading two or more sigma-delta modulators by applying an error signal representing the quantization error of a preceding modulator to a subsequent modulator in the cascade to be quantized therein, the quantized error signal being thereafter differentiated and subtracted from the quantized output signal of the preceding modulator. (col. 1, lines 8-14) The system of FIG. 1 comprises two substantially identical second-order sigma-delta modulators A and B. (col. 3, lines 37-38) X is an analog input signal applied to the system. (col. 4, line 32)

Thus, *Karema et al.* merely discloses second-order sigma-delta modulators A and B. Nothing in *Karema et al.* shows, teaches or suggests a single-stage delta-signal modulator as claimed in claim 1. Rather, *Karema et al.* merely discloses second-order sigma-delta modulators.

Since nothing in *Karema et al.* shows, teaches or suggests a single-stage delta-sigma modulator as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-3 and 5 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 and 5 would not have been anticipated by *Karema et al.* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2-3 and 5 under 35 U.S.C. §102(b).

Claim 11 was rejected under 35 U.S.C. §102(b) as being anticipated by *Walden et al.* (U.S. Patent No. 5,153,593).

Applicants respectfully traverse the Examiner's rejection of the claim under 35 U.S.C. §102(b). The claim has been reviewed in light of the Office Action, and for

reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claim and allows the claim to issue.

*Walden et al.* appears to disclose in FIG. 1 a block diagrammatic representation of the multi-stage sigma-delta analog-to-digital converter 10. The multi-stage converter 10 includes a first sigma-delta converter stage 14 and a second sigma-delta converter stage 18. Although only a two-stage embodiment is depicted in FIG. 1 for the purpose of clarity, it will be apparent from the subsequent discussion that preferred embodiments may be extended to include several or more stages. The first and second stages 14, 18 employ feedback configurations which respectively include first and second integrators 20, 22, first and second M-bit quantizers 24, 26 and first and second M-bit digital to analog converters (DAC's) 28, 30. Electrically connected to the first and second stages are first and second digital noise cancellation networks 31, 32. The second network 32 also contains the digital coefficients c and d. The, coefficients c and d are used to compensate for errors in the analog components, e.g., integrator gain constant, finite operation amplifier gain, etc. (col. 3, lines 37-57) The first stage 14 is disposed to generate a first sequence of digital words representative of the analog input signal X(z). This first digital sequence is then passed through the first digital network 31. In addition, the first integrator 20 accumulates the difference between the analog input signal and the first sequence of digital words, thereby enabling an error signal proportional to the quantization noise associated with the first quantizer 24 to be delivered to an interstage amplifier 34. The interstage amplifier 34 amplifies the error signal so as to utilize the full dynamic range of the second sigma-delta stage 18. The amplified error signal is then quantized by the second stage 18 and processed by the second

noise cancellation network 32 (containing the digital correction coefficients c,d). A interstage digital divider reduces the magnitude of the output from the second noise cancellation network 32 by a factor G equivalent to the gain G of the interstage amplifier 34. The first and second noise cancellation networks 31, 32 are characterized by transfer functions $H_A$ (z) and $H_B$ (z), chosen such that combination of the digital output from the networks 31, 32 at an output summing node 40 results in cancellation of the quantization noise associated with the first stage 14. In this manner the inventive sigma-delta converter 10 is operative to provide a high resolution digital representation of the analog input signal X(z). As shown in FIG. 1, the analog input X(z) is combined at an input summing node 44 with a feedback signal impressed on a feedback line 46 by the first M-bit DAC 28. Coupled to the summing node 44 is the first integrator 20. An analog signal generate by the integrator 20 is provided to the first M-bit A/D converters 24. (col. 3, line 62 through col. 4, line 29) As shown in FIG. 1, the analog input X(z) is combined with the analog signal engendered by the integrator 20 at an interstage summing node 51. This combination produces an error signal substantially identical to first stage quantization noise e.sub.1 delayed by one clock cycle, which is then amplified by an interstage amplifier 34. (col. 4, lines 56-62)

Thus, *Walden et al.* merely discloses that quantizer 24 is provided with the signal generated by integrator 20. Nothing in *Walden et al.* shows, teaches or suggests a multi-bit quantizer which quantizes the analog input signal as claimed in claim 11. Rather, *Walden et al.* merely discloses a quantizer 24 receiving a signal output by an integrator 20. (i.e. quantizer 24 does not receive the analog input X(Z)).

Since nothing in *Walden et al.* shows, teaches or suggests a multi-bit quantizer quantizing an analog input signal as claimed in claim 11, Applicants respectfully request the Examiner withdraws the rejection to claim 11 under 3 U.S.C. §102(b).

Claims 8 and 10 were rejected under 35 U.S.C. §103 as being unpatentable over *Walden et al.* in view of *Karema et al.*

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, *Walden et al.* merely discloses a quantizer 24 receiving an output from an integrator 20. Nothing in *Walden et al.* shows, teaches or suggests a first quantizer quantizing an analog input signal as claimed in claim 8. Rather, *Walden et al.* merely discloses a quantizer 24 receiving a signal generated by integrator 20.

*Karema et al.* as discussed above merely discloses cascading two or more sigma-delta modulator. Nothing in *Karema et al.* shows, teaches or suggests a component separating unit including a first quantizer quantizing an analog input signal as claimed in claim 8. Rather, *Karema et al,* merely discloses cascading two or more sigma-delta modulators.

Since neither *Walden et al.* or *Karema et al.* show, teach or suggest a component separating unit including a first quantizer quantizing an analog input signal as claimed in claim 8, Applicants respectfully request the Examiner withdraws the rejection to claim 8 under 35 U.S.C. §103.

Claim 10 depends from claim 8 and recites an additional feature. Applicants respectfully submit that claim 10 would not have been obvious within the meaning of 35 U.S.C. §103 over *Walden et al.* and *Karema et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 10 under 35 U.S.C. §103.

Since objected to claim 4 depends from an allowable claim, Applicants respectfully request the Examiner withdraws the objection thereto.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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